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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,984	12/28/2001	Yong Jin Cho	8733.563.00	3746
30827	7590	07/12/2005	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP			DI GRAZIO, JEANNE A	
1900 K STREET, NW			ART UNIT	
WASHINGTON, DC 20006			PAPER NUMBER	

2871

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/028,984

Applicant(s)

CHO ET AL.

Examiner

Jeanne A. Di Grazio

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**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on RCE May 16, 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## **DETAILED ACTION**

### ***Claims***

Claims 1-12 are pending per Amendment of April 18, 2005 with claims 1-3, 5 and 8 amended.

### ***Priority***

Priority to Korean Patent Application No. 2001-024581 (May 7, 2001) is claimed.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 18, 2005 has been entered.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 5,668,379 (to Ono et al.)(Published Sept. 16, 1997)(To Hitachi, Ltd.).

Regarding claim 1 (amended), Ono teaches and discloses in all embodiments an active matrix liquid crystal display device comprising a plurality of gate lines formed on an insulating substrate, a plurality of data lines formed so as to cross the plurality of gate lines, thin film transistors formed in the vicinity of respective intersections of the plurality of the gate lines and the data lines and pixel electrodes connected to the thin film transistor (Column 2, “Methods for Solving the Problems”, Lines 23-30)(Applicant’s “a plurality of gate lines on an insulating substrate, a plurality of data lines, and a plurality of TFTs, the gate lines crossing the data lines to define a pixel region and the TFTs being formed at crossing points of the gate and data lines”).

Turning to Figure 16, for example, Ono illustrates a contact hole (pixel electrode region) that electrically connects a source electrode (SD1) of the TFTs with a pixel electrode (d2) of the pixel region is formed over predetermined portions of the source electrode (SD1) and the pixel region and wherein the pixel electrode directly contacts the insulating substrate (SUB1 in pixel electrode region), the source electrode (SD1), and a gate insulating film (GI) contacting a gate electrode (GL (g1)).

Please note that the terms “drain” and “source” are conventionally used interchangeably.

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That is, drain = source and source = drain. Please see, for example, United States Patent 5,838,400 (to Ueda et al.)(Published Nov. 17, 1998)(to Hitachi, Ltd.)(stating “[i]t is, therefore, understood that the source electrode and the drain electrode are switched during operation ... polarity is fixed for convenience, with one of the electrodes taken to be a source electrode and the other a drain electrode.”)(Column 8, Lines 53-61) ; See also, United States Patent 5,528,396 (to Someya et al.)(Published June 18, 1996)(to Hitachi, Ltd.)(stating “the source/drain is, it should be understood, interchangeable during the operation ... one is fixedly expressed as a source, and the other a drain for convenience.”).

As to claim 2 (amended), the gate electrode (GL (g1)) is formed on the insulating substrate (SUB 1), the gate insulating film (GI) formed on the entire surface of the insulating substrate (SUB 1) including the gate electrode (GL (g1)), a semiconductor layer (AS) and an ohmic contact layer (d0) sequentially deposited at a predetermined portion on the gate insulating film (GI) and source and drain electrodes formed right and left (SD1 and DL) on the ohmic contact layer (d0).

Although not shown in Figure 16, a passivation film (PSV1) is formed over the thin film transistor for protecting the thin film transistor from moisture and other contaminants (Column 12, Lines 12-14). Also, please note that layer d1 in Figure 16 is made of chromium and thus a passivation film conventionally covers a chromium layer to protect the chromium film from corrosion. Please see, e.g., United States Patent 5,751,381 (to Ono et al.)(Published May 12, 1998)(to Hitachi, Ltd.)(Column 12, Lines 51-57)(Applicant’s “a passivation film formed on the entire surface of the substrate including the source and drain electrodes, a contact hole formed by etching the passivation film to expose a predetermined portion of the drain electrode and a

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predetermined portion of the insulating substrate, where a pixel electrode will be formed later and the pixel electrode formed on the passivation film and the contact hole.”).

As to claim 3 (amended), Ono teaches and discloses in all embodiments an active matrix liquid crystal display device comprising a plurality of gate lines formed on an insulating substrate, a plurality of data lines formed so as to cross the plurality of gate lines, thin film transistors formed in the vicinity of respective intersections of the plurality of the gate lines and the data lines and pixel electrodes connected to the thin film transistor (Column 2, “Methods for Solving the Problems”, Lines 23-30)(Applicant’s “gate lines arranged to cross data lines on a substrate, thereby defining a pixel region; thin film transistors, each having a gate electrode and source and drain electrodes, formed at crossing points of the gate lines and the data lines;”.)

Turning to Figure 16, for example, Ono illustrates a contact hole (pixel electrode region) that electrically connects a source electrode (SD1) of the TFTs with a pixel electrode (d2) of the pixel region is formed over predetermined portions of the source electrode (SD1) and the pixel region and wherein the pixel electrode directly contacts the insulating substrate (SUB1 in pixel electrode region), the source electrode (SD1), and a gate insulating film (GI) contacting a gate electrode (GL (g1)).

Please note that the terms “drain” and “source” are conventionally used interchangeably.

That is, drain = source and source = drain. Please see, for example, United States Patent 5,838,400 (to Ueda et al.)(Published Nov. 17, 1998)(to Hitachi, Ltd.)(stating “[i]t is, therefore, understood that the source electrode and the drain electrode are switched during operation ... polarity is fixed for convenience, with one of the electrodes taken to be a source electrode and the other a drain electrode.”)(Column 8, Lines 53-61) ; See also, United States Patent 5,528,396

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(to Someya et al.)(Published June 18, 1996)(to Hitachi, Ltd.)(stating “the source/drain is, it should be understood, interchangeable during the operation ... one is fixedly expressed as a source, and the other a drain for convenience.”).

As to claim 4, the contact hole of Figure 16 is formed over an edge part of the source electrode and the pixel region adjacent to an edge part of the source electrode.

Figure 16, shows the contact hole traced over part of the source electrode and into the pixel region.

As to claim 5 (amended), the gate electrode (GL (g1)) is formed on the insulating substrate (SUB 1), the gate insulating film (GI) formed on the entire surface of the insulating substrate (SUB 1) including the gate electrode (GL (g1)), a semiconductor layer (AS) on the gate insulating film (GI) above the gate electrode (GL(g1)), source (SD1) and drain (DL) electrodes located at opposite sides of the semiconductor layer (AS).

Although not shown in Figure 16, a passivation film (PSV1) is formed over the thin film transistor for protecting the thin film transistor from moisture and other contaminants (Column 12, Lines 12-14). Also, please note that layer d1 in Figure 16 is made of chromium and thus a passivation film conventionally covers a chromium layer to protect the chromium film from corrosion. Please see, e.g., United States Patent 5,751,381 (to Ono et al.)(Published May 12, 1998)(to Hitachi, Ltd.)(Column 12, Lines 51-57)(Applicant’s “a passivation film formed on the entire surface of the substrate including the source and drain electrodes.”).

As to claims 6 and 7, the contact hole of Figure 16 is formed over an edge part of the source electrode and the pixel region adjacent to an edge part of the source electrode.

Figure 16, shows the contact hole traced over part of the source electrode and into the pixel region.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8-12 rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,668,379 (to Ono et al.)(Published Sept. 16, 1997)(To Hitachi, Ltd.).

As to claims 8-12 (claim 8 being amended), the method for fabricating the liquid crystal display device would have been obvious in view of the active matrix liquid crystal display device as taught and disclosed in Ono for a display having a bright image and preferable production yield (Abstract and entire patent).



*Response to Arguments*

Applicant's arguments with respect to said claims have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio  
Patent Examiner  
Art Unit 2871

JDG



DUNG T. NGUYEN  
PRIMARY EXAMINER